CLAIMS

Please amend the claims as follows.

1. (Currently Amended) An M-bit adder capable of receiving a first M-bit argument, a second M-bit argument, and a carry-in (CI) bit comprising:

M adder cells arranged in R rows, wherein a least significant adder cell in a first one of said rows of adder cells is operable to:

receive [[s]] a first data bit, A_X, from said first M-bit argument and a first data bit, B_X, from said second M-bit argument, ~~and~~

generate [[s]] both a first conditional carry-out bit, $C_X(1)$, and a second conditional carry-out bit, $C_X(0)$, and

provide the first and second conditional carry-out bits to another of said adder cells,

wherein said $C_X(1)$ bit is calculated assuming a row carry-out bit from a second row of adder cells preceding said first row is a 1 and said $C_X(0)$ bit is calculated assuming said row carry-out bit from said second row is a 0.

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2. (Original) The M-bit adder as set forth in Claim 1 wherein said least significant adder cell generates a first conditional sum bit, $S_X(1)$, and a second conditional sum bit, $S_X(0)$.

3. (Original) The M-bit adder as set forth in Claim 2 wherein said $S_X(1)$ bit is calculated assuming said row carry-out bit from said second row is a 1 and said $S_X(0)$ bit is calculated assuming said row carry-out bit from said second row is a 0.

4. (Original) The M-bit adder as set forth in Claim 3 wherein said row carry-out bit selects one of said $S_X(1)$ bit and said $S_X(0)$ bit to be output by said least significant adder cell.

5. (Original) The M-bit adder as set forth in Claim 4 wherein said first row of adder cells further comprises a second adder cell coupled to said least significant adder cell, wherein said second adder cell receives a second data bit, A_{X+1}, from said first M-bit argument and a second data bit, B_{X+1}, from said second M-bit argument, and receives from said least significant adder cell said $C_X(1)$ bit and said $C_X(0)$ bit.

6. (Original) The M-bit adder as set forth in Claim 5 wherein said second adder cell generates a first conditional carry-out bit, $C_{X+1}(1)$, wherein said $C_{X+1}(1)$ bit is generated from said A_{X+1} data bit, said B_{X+1} data bit, and said $C_X(1)$ bit from said least significant adder cell.

7. (Original) The M-bit adder as set forth in Claim 6 wherein said second adder cell generates a second conditional carry-out bit, $C_{X+1}(0)$, wherein said $C_{X+1}(0)$ bit is generated from said A_{X+1} data bit, said B_{X+1} data bit, and said $C_X(0)$ bit from said least significant adder cell.

8. (Original) The M-bit adder as set forth in Claim 7 wherein said second adder cell generates a first conditional sum bit, $S_{X+1}(1)$, wherein said $S_{X+1}(1)$ bit is generated from said A_{X+1} data bit, said B_{X+1} data bit, and said $C_X(1)$ bit from said least significant adder cell.

9. (Original) The M-bit adder as set forth in Claim 8 wherein said second adder cell generates a second conditional sum bit, $S_{X+1}(0)$, wherein said $S_{X+1}(0)$ bit is generated from said A_{X+1} data bit, said B_{X+1} data bit, and said $C_X(0)$ bit from said least significant adder cell.

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10. (Original) The M-bit adder as set forth in Claim 9 wherein said row carry-out bit selects one of said $S_{X+1}(1)$ bit and said $S_{X+1}(0)$ bit to be output by said second adder cell.

11. (Original) The M-bit adder as set forth in Claim 1 wherein said first row of adder cells contains N adder cells and said second row of adder cells preceding said first row contains less than N adder cells.

12. (Currently Amended) A data processor comprising:

an instruction execution pipeline comprising N processing stages, each of said N processing stages capable of performing one of a plurality of execution steps associated with a pending instruction being executed by said instruction execution pipeline, wherein at least one of said N processing stages comprises an M-bit adder capable of receiving a first M-bit argument, a second M-bit argument, and a carry-in (CI) bit, said M-bit adder comprising:

M adder cells arranged in R rows, wherein a least significant adder cell in a first one of said rows of adder cells is operable to:

receive [[s]] a first data bit, A_X, from said first M-bit argument and a first data bit, B_X, from said second M-bit argument, ~~and~~

generate [[s]] both a first conditional carry-out bit, $C_X(1)$, and a second conditional carry-out bit, $C_X(0)$, and

provide the first and second conditional carry-out bits to another of said adder cells,

wherein said $C_X(1)$ bit is calculated assuming a row carry-out bit from a second row of adder cells preceding said first row is a 1 and said $C_X(0)$ bit is calculated assuming said row carry-out bit from said second row is a 0.

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13. (Original) The data processor as set forth in Claim 12 wherein said least significant adder cell generates a first conditional sum bit, $S_X(1)$, and a second conditional sum bit, $S_X(0)$.

14. (Original) The data processor as set forth in Claim 13 wherein said $S_X(1)$ bit is calculated assuming said row carry-out bit from said second row is a 1 and said $S_X(0)$ bit is calculated assuming said row carry-out bit from said second row is a 0.

15. (Original) The data processor as set forth in Claim 14 wherein said row carry-out bit selects one of said $S_X(1)$ bit and said $S_X(0)$ bit to be output by said least significant adder cell.

16. (Original) The data processor as set forth in Claim 15 wherein said first row of adder cells further comprises a second adder cell coupled to said least significant adder cell, wherein said second adder cell receives a second data bit, A_{X+1}, from said first M-bit argument and a second data bit, B_{X+1}, from said second M-bit argument, and receives from said least significant adder cell said $C_X(1)$ bit and said $C_X(0)$ bit.

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17. (Original) The data processor as set forth in Claim 16 wherein said second adder cell generates a first conditional carry-out bit, $C_{X+1}(1)$, wherein said $C_{X+1}(1)$ bit is generated from said A_{X+1} data bit, said B_{X+1} data bit, and said $C_X(1)$ bit from said least significant adder cell.

18. (Original) The data processor as set forth in Claim 17 wherein said second adder cell generates a second conditional carry-out bit, $C_{X+1}(0)$, wherein said $C_{X+1}(0)$ bit is generated from said A_{X+1} data bit, said B_{X+1} data bit, and said $C_X(0)$ bit from said least significant adder cell.

19. (Original) The data processor as set forth in Claim 18 wherein said second adder cell generates a first conditional sum bit, $S_{X+1}(1)$, wherein said $S_{X+1}(1)$ bit is generated from said A_{X+1} data bit, said B_{X+1} data bit, and said $C_X(1)$ bit from said least significant adder cell.

20. (Original) The data processor as set forth in Claim 19 wherein said second adder cell generates a second conditional sum bit, $S_{X+1}(0)$, wherein said $S_{X+1}(0)$ bit is generated from said A_{X+1} data bit, said B_{X+1} data bit, and said $C_X(0)$ bit from said least significant adder cell.

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21. (Original) The data processor as set forth in Claim 20 wherein said row carry-out bit selects one of said $S_{X+1}(1)$ bit and said $S_{X+1}(0)$ bit to be output by said second adder cell.

22. (Original) The data processor as set forth in Claim 12 wherein said first row of adder cells contains N adder cells and said second row of adder cells preceding said first row contains less than N adder cells.

23. (Original) A method of adding a first M-bit argument and a second M-bit argument in an M-bit adder, the M-bit adder comprising M adder cells arranged in R rows, the method comprising the steps of:

receiving a first data bit, A_X, from the first M-bit argument and a first data bit, B_X, from the second M-bit argument in a least significant adder cell in a first one of the rows of adder cells;

calculating in the least significant adder cell a first conditional carry-out bit, $C_X(1)$, assuming a row carry-out bit from a second row of adder cells preceding the first row is a 1;

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calculating in the least significant adder cell a second conditional carry-out bit, $C_X(0)$, assuming the row carry-out bit from the second row is a 0;

calculating in the least significant adder cell a first conditional sum bit, $S_X(1)$, assuming the row carry-out bit from the second row is a 1;

calculating in the least significant adder cell a second conditional sum bit, $S_X(0)$, assuming the row carry-out bit from the second row is a 0;

propagating the $C_X(1)$ bit and the $C_X(0)$ bit to a second adder cell in the first row of adder cells; and

selecting one of the $S_X(1)$ bit and the $S_X(0)$ bit to be output from the least significant adder cell according to a value of the row carry-out bit from the second row.